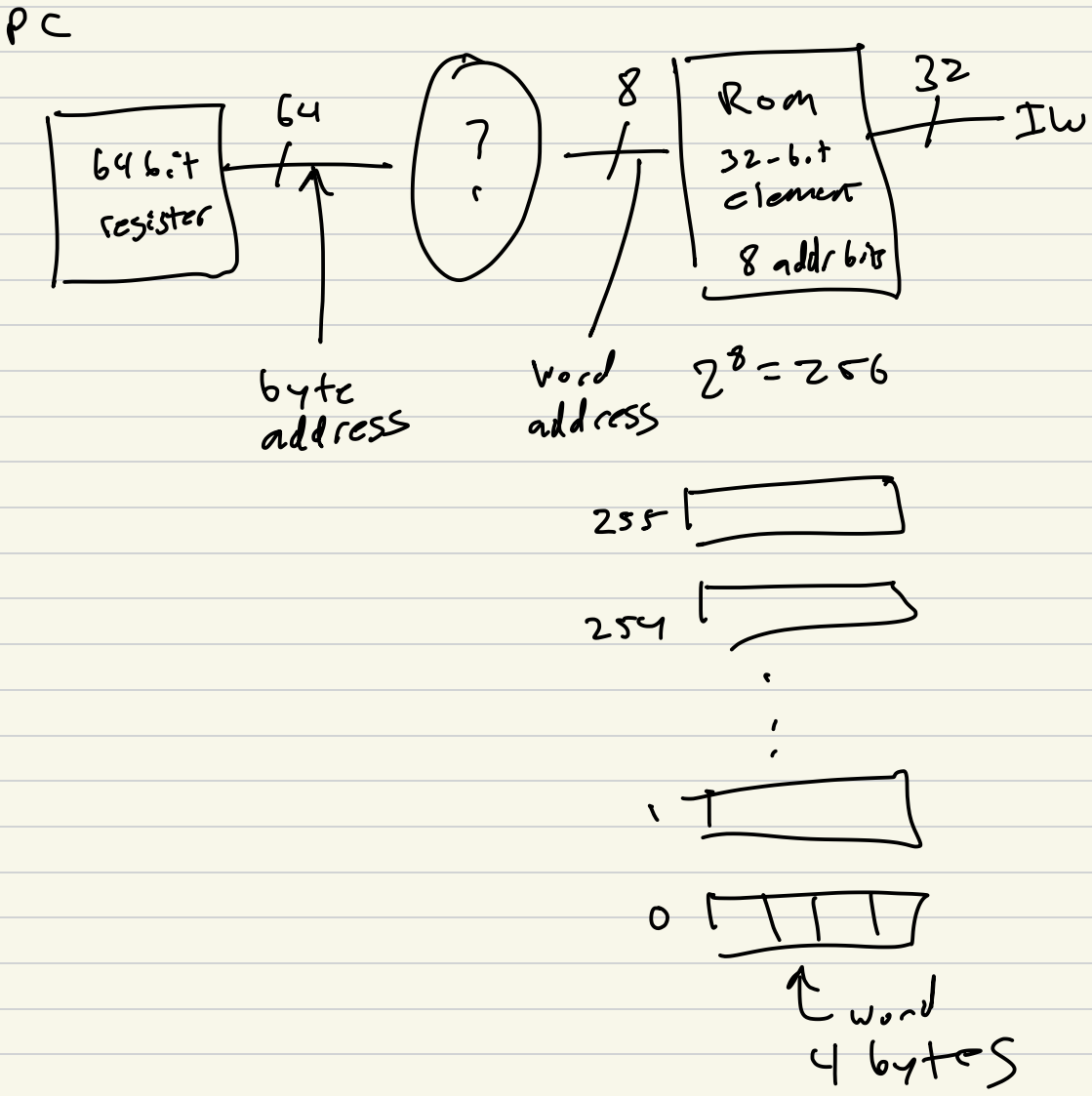
CS 315-02 Processor Decoding 2025-10-30

Lab09 testing

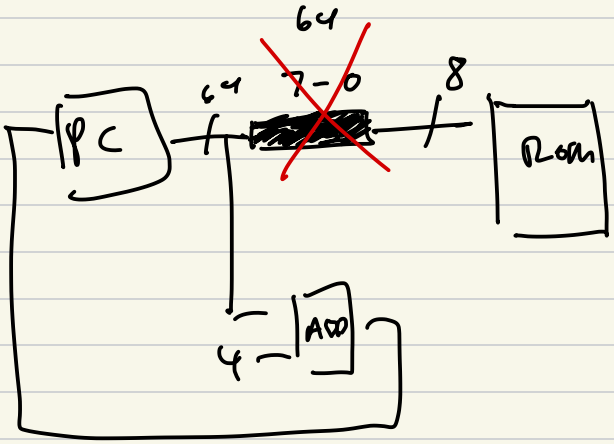


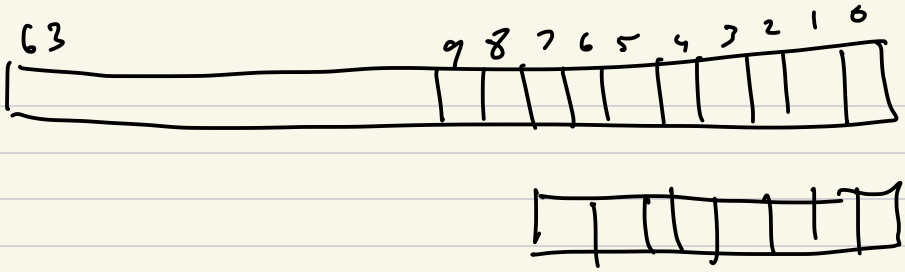
Memory

addr_byte

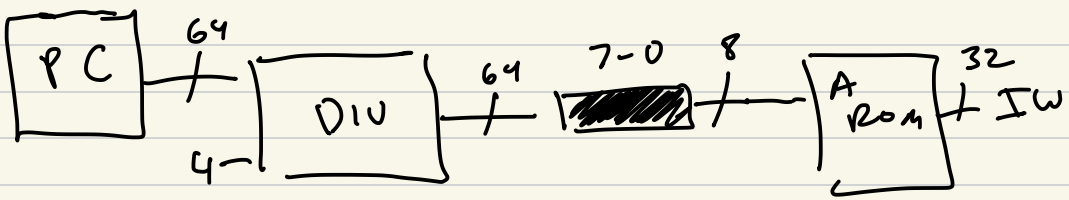
addr_word = addr_byte / 4

addr_word = addr_byte >> 2

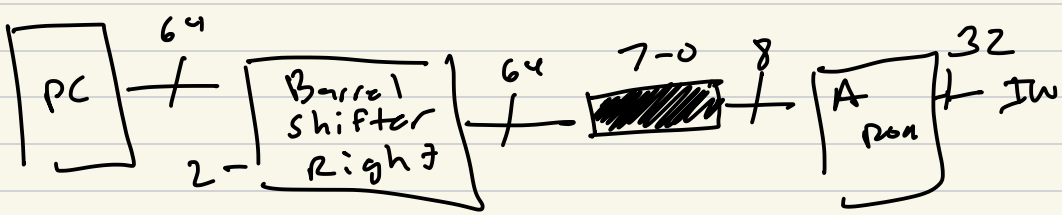



63
9 8 7 6 5 4 3 2 1 0

(1)

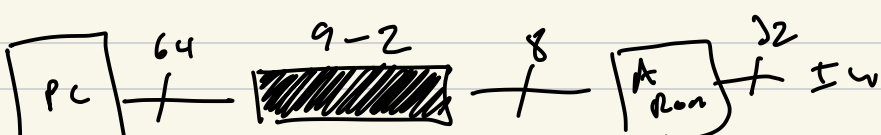

PC
64
4
DIV
64
7-0
8
A
ROM
32
IW

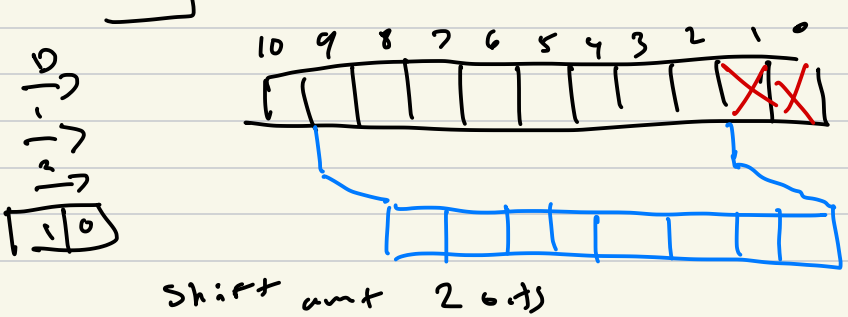
(2)

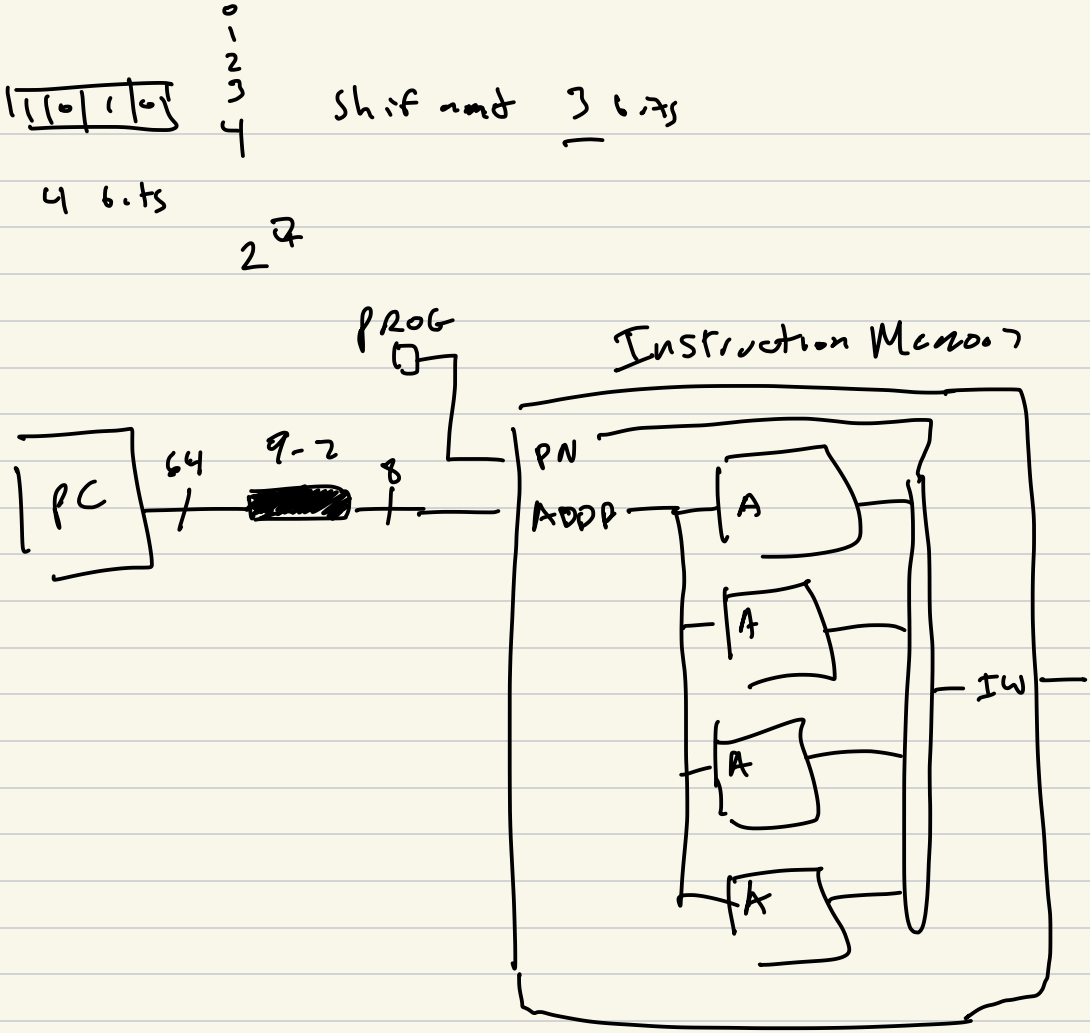

PC
64
2
Barrel
shifter
Right
64
7-0
8
A
ROM
32
IW

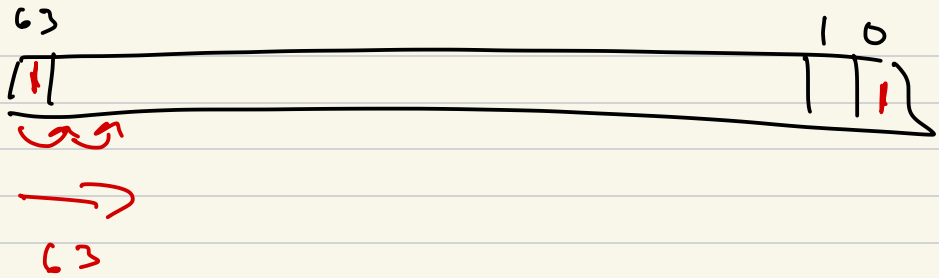
*

(3)

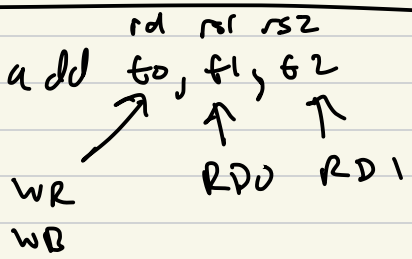

PC
64
9-2
8
A
ROM
32
IW

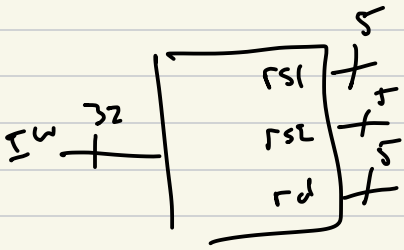

10 9 8 7 6 5 4 3 2 1 0
0
1
2
1 0
shift amt 2 bits

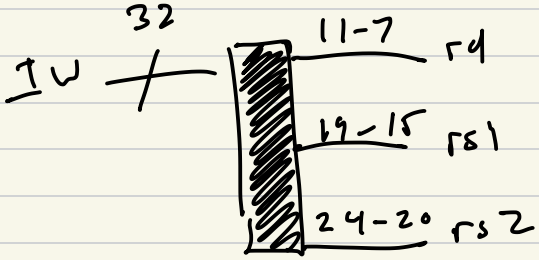

0
1
2
3
4
Shift amt 3 bits
4 bits
2^4
PROG
Instruction Memory
PC
64
9-2
8
PN
ADDR
A
A
A
A
IW


63
1 0
63

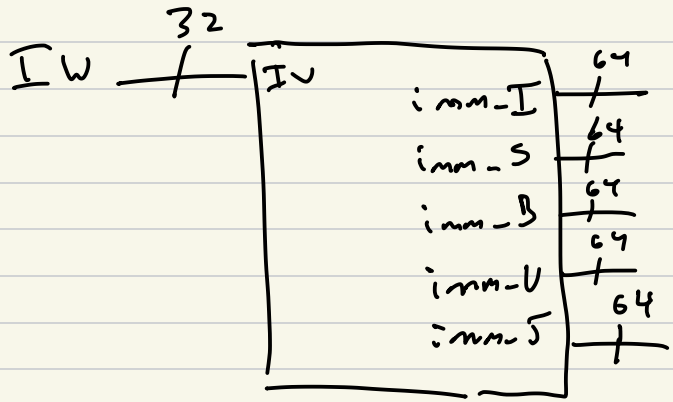
Reg Decoder

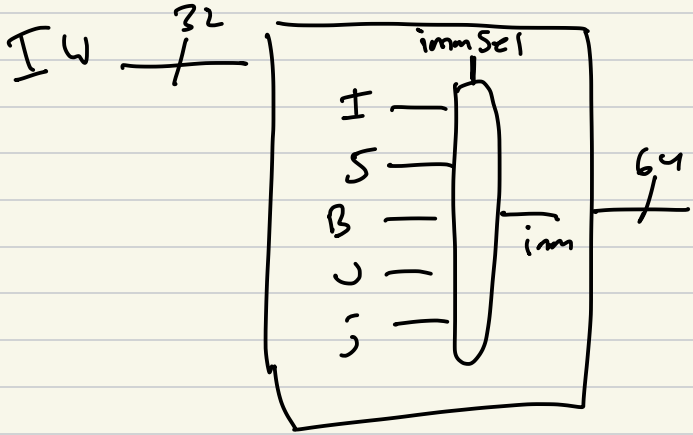

rd rs1 rs2
add t0, t1, t2
WR
WB
RD0
RD1


IW
32
rs1
rs2
rd
5
5
5

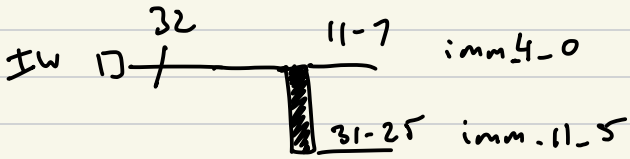

IW
32
11-7
rd
19-15
rs1
24-20
rs2

Immediate Decoder

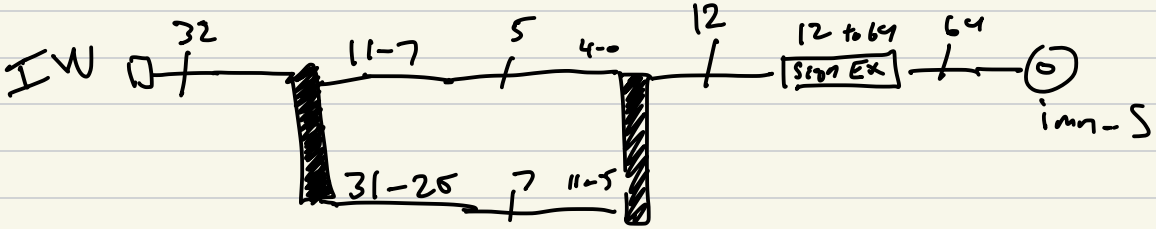




S-Type Immediate



Goal: construct a 64 bit signed value



How to implement the sign extender